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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/846,462 | 05/01/2001 | Jia-Shyong Cheng | 55733 | 4634 |

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EXAMINER

SCHECHTER, ANDREW M

ART UNIT PAPER NUMBER

2871

DATE MAILED: 07/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/846,462

Applicant(s)

CHENG ET AL.

Examiner

Andrew Schechter

Art Unit

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 April 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) 19-28 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-10 and 12-18 is/are rejected.
- 7) ☒ Claim(s) 4 and 11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Claim Objections

1. Claims 1, 7, and 15 are objected to because of the following informalities:
Claims 2 and 4 refer to "said gate conductive line" while claim 1 recites a "gate conductive structure". Claim 7 recites a "said insulation layer" while claim 1 recites a "gate insulation layer". Claim 15 recites a "said data electrode and said pixel portions of said common electrode are exposed", while it appears that "said pixel portions of said data electrode and said common electrode are exposed" is intended. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3, 7-10, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Kim*, U.S. Patent No. 6,177,970 in view of *Kim et al.*, U.S. Patent No. 5,917,564.

Kim '970 discloses [see Figs. 4-5, for instance] a process for forming an in-plane switching mode liquid crystal display (IPS-LCS) comprising steps of: providing an insulating substrate [10], forming a first conductive layer [20, 30, 210] on a first side of

said substrate, and defining a gate conductive structure [20, 210] and a bus portion of a common electrode [30]; forming a gate insulating layer [50] and a semiconductor layer [60 (misabeled in Fig. 5)]; defining a contact via [520] for interconnection to said bus portion of said common electrode; forming a second conductive layer [40, 70, 310, 710, 720] and defining source/drain regions [710, 720], a data line [70], a pixel portion of a data electrode [40], and a pixel portion of a common electrode [310], with said gate insulation layer as a stopper [see Fig. 5]; wherein said pixel portion of said common electrode is interconnected to said bus portion of said common electrode through said contact via; and forming a passivation layer [80] and defining a pixel region for exposing said pixel portions of said data and common electrodes [region (a)].

Kim '970 does not disclose completing the tri-layer structure with an etch stopper layer, defining an etch stopper structure with a portion of said semiconductor layer exposed, forming a highly doped semiconductor layer [though *Kim '907* does disclose an equivalent ohmic contact layer [611 and 612] without explicitly stating that it is a highly doped semiconductor layer], and having the said etch stopper structure as a stopper with the gate insulation layer. In other words, *Kim '970* does not disclose the transistor having an etch stopper and highly doped semiconductor layer.

Kim '564 discloses [see Fig 5b, etc.] just such an transistor having an etch stopper and highly doped semiconductor layer, for an analogous IPS-LCD device. This includes the tri-layer structure of gate insulating layer [12], semiconductor layer [13], and etch stopper layer [14]; defining an etch stopper structure with a portion of the semiconductor layer exposed [see Fig. 5b], forming a highly-doped semiconductor layer

[16], and defining the various electrodes using the etch stopper structure and the gate insulation layer as a stopper. *Kim '564* teaches the advantage of having the etch stopper layer, saying "The channel protection layer [etch stopper] is designed to protect the channel portion of the active region in the first amorphous semiconductor layer from potential damage which may occur during subsequent process steps" [col. 3, lines 48-51]. *Kim '564* also teaches the advantage of having the highly doped semiconductor layer, saying "As will be understood by those skilled in the art, the relatively highly doped amorphous semiconductor layer 16 provides a low resistance intermediate contact between the first amorphous semiconductor layer 13 and the second conductive layer" [col. 6, lines 35-39]. It would therefore have been obvious to one of ordinary skill in the art to use the etch stopper and the highly-doped semiconductor layer of *Kim '564* in the device of *Kim '970*, motivated by the teachings of *Kim '564*. Claim 1 is therefore unpatentable.

A storage-capacitor portion of the common electrode [the parts of the common bus line in Fig. 4 which the pixel portion of the data electrode overlap the common electrode] is simultaneously defined together with the gate conductive line and the bus portion of the common electrode, so claim 2 is also unpatentable. A storage-capacitor portion of the data electrode [the parts of the data electrode lines in Fig. 4 which extend over the common electrode bus line] is simultaneously defined together with the source/drain regions, data line, and pixel portions, so claim 3 is also unpatentable.

The gate insulation layer [50] is made of silicon nitride [col. 4, line 3], so claim 7 is also unpatentable. The etch stopper layer [14] is made of silicon nitride [col. 2, line

15-16], so claim 8 is also unpatentable. The semiconductor layer is intrinsic amorphous silicon [col. 4, line 4], so claim 9 is also unpatentable. The highly doped amorphous semiconductor layer [16] is highly doped amorphous silicon [col. 6, line 28], so claim 10 is also unpatentable. The passivation layer is formed of silicon nitride [col. 4, lines 16-17], so claim 12 is also unpatentable. Neither reference explicitly states that the insulating substrate is a transparent glass; the examiner takes official notice that using transparent glass as the substrate in this type of LCD is well-known and conventional, so it would have been obvious to one of ordinary skill in the art to do so, motivated by the manufacturing convenience of using established processes with the conventional material for this component. Claim 13 is therefore unpatentable.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Kim*, U.S. Patent No. 6,177,970 in view of *Kim et al.*, U.S. Patent No. 5,917,564, as applied to claim 1 above, in view of *Kim*, U.S. Patent No. 6,177,970.

Considering claim 5, Fig. 4 of *Kim '970* shows the pixel portion of the data electrode having a comb shape, but the pixel portion of the common electrode being three separate segments. However, having it this way is just an art-recognized equivalent to having both comb-shaped, as *Kim '970* teaches that "a plurality of the pixel and common electrodes 40 and 310 may be formed in a single body by adding a pixel connection portion and a common connection, and single contact holes are formed in this case" [col. 4, lines 56-60]. It would therefore be obvious to one of ordinary skill in the art to have the pixel portion of the common electrode having a comb shape, motivated by the art-recognized equivalence of the two setups. (In both cases, the

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electrodes are arranged opposite each other with alternate comb teeth.) Claim 5 is therefore unpatentable.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Kim*, U.S. Patent No. 6,177,970 in view of *Kim et al.*, U.S. Patent No. 5,917,564, as applied to claim 1 above, in view of *Kim et al.*, U.S. Patent No. 5,907,379.

Kim '970 discloses that the first conductive layer is a metal [col. 3, line 65], but is silent on which metal is used. *Kim '379* discloses using aluminum, chromium, or molybdenum, and teaches that using aluminum "is desirable in view of the aperture ratio" [col. 4, lines 3-8]. It would have been obvious to one of ordinary skill in the art to do so in *Kim '970*, motivated by this teaching of *Kim '379*. Claim 6 is therefore unpatentable.

6. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Kim*, U.S. Patent No. 6,177,970 in view of *Kim et al.*, U.S. Patent No. 5,917,564, as applied to claim 1 above, in view of *Yun et al.*, U.S. Patent No. 6,486,934. (*Yun* was filed on 15 December 2000, so this rejection might be overcome by the filing of a certified translation of the applicant's priority document.)

Kim '970 and *Kim '564* do not disclose having the second conductive layer be a composite metal on transparent electrode, removing a portion of the metal layer in the pixel region, the metal layer being Mo, Al, or Mo/Al/Mo, and the transparent electrode layer being indium tin oxide. *Yun* does disclose all this [see Figs. 2D, 2E, etc.] and it would be obvious to one of ordinary skill in the art to do so in the above device, motivated by *Yun's* teaching that this obtains a double layer structure for the data line

[thus reducing electrical resistance, improving signal quality and display quality] while providing a transparent pixel electrode in the pixel region [allowing for high aperture ratio and good brightness]. Claims 14-17 are therefore unpatentable.

7. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Kim*, U.S. Patent No. 6,177,970 in view of *Kim et al.*, U.S. Patent No. 5,917,564 and *Yun et al.*, U.S. Patent No. 6,486,934 as applied to claim 15 above, and further in view of *Ozaki*, U.S. Patent No. 6,469,769 and *Oh et al.*, U.S. Patent No. 6,130,729. (*Yun* was filed on 15 December 2000, so this rejection might be overcome by the filing of a certified translation of the applicant's priority document.)

Kim '970 and *Kim '564* do not disclose the back-exposure method of defining the etch stopper recited in claim 18. *Ozaki* does disclose it [see abstract, for instance], as does *Oh* [abstract, etc.], and it would be obvious to one of ordinary skill in the art to use this back-exposure method, motivated by *Oh*'s teaching that it avoids the necessity of an additional pattern mask [and thereby simplifies the manufacturing process], and *Ozaki*'s teaching that it produces the etch-stopper in "a self-aligned manner" [col. 2, line 45] which improves the quality of the display by avoiding alignment errors and simplifies the process by avoiding a required alignment step. Claim 18 is therefore unpatentable.

Allowable Subject Matter

8. Claims 4 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 14-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if the rejections in view of *Yun* are overcome as discussed above.

10. The following is a statement of reasons for the indication of allowable subject matter:

Claim 4 adds the limitation that the storage capacitor is between the pixel region and the said gate conductive line. Fig. 4 of *Kim '970* shows the storage capacitor between the pixel region and the neighboring gate conductive line, rather than the said gate conductive line (it is on the other side of the pixel). Fig. 1 of *Kim '970* shows an embodiment in which a storage-capacitor is disposed between a boundary of the pixel region and the gate conductive line as recited by claim 4, but does not have the feature that the storage capacitor portion of the common electrode is formed with the gate conductive line, or that the storage capacitor portion of the data electrode is formed with the pixel portions of the data electrode, as required by claims 2 and 3. There is no suggestion or motivation in the prior art for extending an electrode from the common bus line to the side of pixel next to the said gate conductive line, so it would not be an obvious modification of any of the embodiments of *Kim '970* to obtain a device which satisfies the limitations of claim 4 as well as the limitations of claims 1-3. Claim 4 would therefore be allowable if rewritten appropriately.

Claim 11 recites the additional limitation that the second conductive layer (including the data line) is formed of ITO, IZO, or IPbO. *Kim '970* discloses making the

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second conductive layer of a metal [col. 4, line 10] and discusses that the resistance of the data line may be too large [col. 5, lines 45-50]. It would therefore not be an obvious modification to one of ordinary skill in the art to replace the metal with ITO, IZO, or IPbO, which have higher resistances than the metals (such as those listed in claim 6) which *Kim '970* would be using for the data line. Claim 11 would therefore be allowable if rewritten appropriately.

The prior art other than *Yun* does not disclose or suggest the device of claim 1 with the additional limitation of claim 14 that the second conductive layer is a composite with metal overlying a transparent electrode. Claim 14, and its dependent claims 15-18, would therefore be allowable if rewritten appropriately.

Election/Restrictions

11. Applicant's election without traverse of Group I, claims 1-18, in Paper No. 5 is acknowledged. Claims 19-28 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group, there being no allowable generic or linking claim.

Conclusion


12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.


U.S. Patent No. 5,907,379 to *Kim et al.* discloses an IPS-LCD with pixel electrodes in which an ITO layer is on top of a metal layer, rather than metal on top of an ITO layer, as in claim 14.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (703) 306-5801. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (703) 305-3492. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-4711 for regular communications and (703) 746-4711 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.


Andrew Schechter
June 26, 2003


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